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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/674,444

10/31/2000

Symon Reuben Brewer

20251-000100

9030

7590

10/28/2005

Townsend And Townsend And Crew
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Denver, CO 80202-5827

EXAMINER

FILE, ERIN M

ART UNIT

PAPER NUMBER

2634

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/674,444	BREWER, SYMON REUBEN	
	Examiner	Art Unit	
	Erin M. File	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) 1-3,5-12 and 15-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3,5-12 and 15-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 October 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2, 5-11, 15-17, 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shohet and in view of Lee.

Claims 1, 10, 11, Shohet discloses forming an offset reference clock signal being offset by a predetermined frequency amount from said digital signal; (column 4, lines 50-65, fig 1., fig 2) and sampling said digital signal at sampling times determined by an integer multiple of the frequency of said offset reference clock signal, such that, in the absence of jitter and said offset by a predetermined frequency, there are a predetermined number of sampling times in each bit of said digital signal; (column 4, lines 50-65), fig 1., fig 2 detecting occasions when the number of sampling times in any bit of said digital signal is different from said predetermined number; Abstract counting said occasions over a predetermined time, and fig 1, Abstract deriving at least one measure of jitter from said counting of said occasions (Column 3, Lines 50-54). Shohet fails to disclose

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the offset reference clock signal moving relative to a transition point for bits of the digital signal. However, Lee discloses the creation of an output pulse train responding to transitions in the received digital data signal (col. 2, lines 46-48). Because Lee discloses that the creation of this pulse train is for synchronization purposes, which improve the ability make accurate measurements, it would be obvious to one skilled in the art at the time of invention to incorporate Lee's disclosure into Shohet's jitter measurement device.

Claims 2, 17, Shohet discloses wherein said offset reference clock signal is formed by extracting a clock signal from said digital signal and offsetting said clock signal by said predetermined frequency (Column 1, lines 39- 44).

Claim 5, 16, 20, Shohet discloses sampling the times are at clock bit intervals being plus and minus one of said integer multiple (Fig. 2)

Claims 6, 15, 19, contain the limitations of Claim 1, although both Lee and Shohet fail to disclose the method of determining a sampling period, using the inverse proportion of the bit rate and higher frequency offset is a design choice and simply represents using the original clock frequency (bit rate) and some offset.

Claims 7, 21, Shohet meets the following limitations of the Claim: wherein one of said at least one measure of jitter is obtained by counting up one value for each of said

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occasions representing sampling times greater than the predetermined number within a bit, counting down one value for each of said occasions representing sampling times less than the predetermined number within a bit and determining the difference between the maximum count value and the minimum count value. Abstract; (Column 3, lines S6-65)

Claims 8, 22, Shohet meets the following limitations of the Claim: wherein one of said at least one measure of jitter is obtained by counting up one value for each of said occasions representing sampling times greater than the predetermined number within a bit, counting down one value for each of said occasions representing sampling times less than the predetermined number within a bit and determining the time difference between the first occasion of the maximum count value and the last occasion of the minimum count value. Abstract; (Column 3, lines 56-60)

Claims 9, 23, Shohet meets the following limitations of the Claim: wherein the time difference is divided by said integer multiple and said predetermined time. fig 2: fig 1, item 22, 24: (Column 4, Lines 11-12)

3. Claims 3, 12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shohet and Lee and in further view of Yoshimura et al.

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Claims 3, 12, 18, inherit the limitations of Claims 1, 11, and 17 respectively. Both Shohet and Lee fail to smoothing of the reference clock. However, Yoshimura discloses "a phase comparator (5) for calculating a phase difference by using sampled values before and after an edge portion of the signals outputted from the A/D converter (4), a filter (6) for smoothing the phase difference outputted from the phase comparator (5) so as to output a signal converted into a direct current, a variable frequency oscillator (7) for reproducing a synchronous clock on the basis of the signal-outputted from the filter (6), a jitter measuring section 9 for detecting a jitter detection signal on the basis of unevenness of the phase difference obtained by the phase comparator (5)" (col. 3, lines 12-24). Because smoothing the reference clock can result in more accurate phase measurements, resulting in improved jitter measurement, it would be obvious to one skilled in the art at the time of invention to incorporate the clock smoothing of Toshimura in to the combined invention of Shohet and Lee.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin M. File whose telephone number is (571)272-6040. The examiner can normally be reached on M-F 9:30-6:00.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571)272-3056. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erin M. File

EF

10/21/2005


STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600